IN THE CLAIMS

1. (Previously Amended) A content addressable memory (CAM) system including an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group, wherein during compare operations between a comparand word and data stored in the array group the mask pattern masks the comparand word and is not compared with the data stored in the array group.

2. (Original) The CAM system of Claim 1, wherein two or more array groups have the same priority.

3. (Original) The CAM system of Claim 1, wherein the priority comprises a prefix of a classless inter-domain routing (CIDR) address.

4. (Original) The CAM system of Claim 3, further comprising:

means for generating an index of the longest prefix match in response to a comparison between a search key and data stored in the array groups.

5. (Original) The CAM system of Claim 3, further comprising:

means for storing data in the array groups according to prefix.

6. (Original) The CAM system of Claim 1, further comprising:

means for selectively comparing a search key with data stored in the array groups according to priority.

7. (Original) The CAM system of Claim 6, wherein the means for selectively comparing comprises:

means for receiving a priority for the search key; and

means for comparing the search key with data stored only in the array groups that have the same priority as the search key.

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~~8.~~ (Twice Amended) A content addressable memory (CAM) system, comprising:

an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group;

means for comparing ~~the~~ a search key with data stored in the array groups;

means for comparing a priority of the search key with the priority of each array group; and

means for selectively enabling results of the comparison of the search key and the data in each array group in response to the comparison of their priorities.

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~~9.~~ (Original) The CAM system of Claim ~~8~~, wherein the means for comparing the priorities includes a priority table for storing the priority of each array group.

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~~10.~~ (Twice Amended) A content addressable memory (CAM) system, comprising:

an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group;

a select circuit having a plurality of inputs to receive match signals from the plurality of array groups during a compare operation between ~~the~~ a search key and data stored in the array groups, and having a plurality of outputs to provide

qualified match signals for the plurality of array groups; and

a priority encoder having a plurality of inputs to receive the plurality of qualified match signals, and having an output to generate an index of the highest priority match in response to the qualified match signals.

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~~11~~. (Original) The CAM system of Claim ~~10~~, wherein the select circuit includes means for selectively forcing the qualified match signals to a mismatch state according to priority.

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~~12~~. (Original) The CAM system of Claim ~~10~~, wherein the select circuit passes only the match signals from array groups having the same priority as the search key, while disqualifying the match signals from other array groups.

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~~13~~. (Original) The CAM system of Claim ~~10~~, wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the match signals from a corresponding array group, a second input to receive an enable signal for the corresponding array group, and outputs to selectively provide the match signals to the priority encoder as qualified match signals in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priority of the search key and the priorities of the array groups.

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~~14~~. (Original) The CAM system of Claim ~~13~~, wherein the compare circuit further comprises a priority table having a plurality of rows, each for storing the priority of a corresponding array group.

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~~15~~. (Original) The CAM system of Claim ~~14~~ 20, wherein the select circuit further comprises a plurality of group match flag circuits, each receiving the match signals from a corresponding array group and generating a group match flag in response thereto, wherein the group match flags are provided as select signals to corresponding rows of the priority table.

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~~16~~. (Original) The CAM system of Claim 1, further comprising:

means for storing data in the array groups according to priority.

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~~17~~. (Twice Amended) The CAM system of Claim ~~21~~ ~~16~~, wherein the means for storing comprises an address circuit having a first input to receive the priority of the data, a second input to receive a next free address (NFA) corresponding to the priority, and having outputs coupled to the array groups.

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~~18~~. (Original) The CAM system of Claim ~~17~~, wherein the address circuit comprises an address decoder to select a row in one array group corresponding to the priority in response to the NFA.

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~~19~~. (Original) The CAM system of Claim ~~18~~, wherein the address circuit further comprises an NFA table having a number of rows, each row for storing the NFA for a corresponding priority.

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~~20~~. (Original) The CAM system of Claim ~~19~~, wherein each row in the NFA table includes an empty bit indicative of whether any array group is assigned to the corresponding

priority.

21-22. (Canceled)

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~~23~~. (Currently Amended) ~~The CAM system of Claim 22,~~ A content addressable memory (CAM) system, comprising:

an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group;

and

an index circuit to generate a next free address (NFA) for the data according to its priority, wherein the index circuit comprises:

a select circuit having a plurality of inputs to receive valid bits from the plurality of array groups, the valid bits indicating whether valid data is stored in corresponding rows of the array group, and having a plurality of outputs to provide qualified valid bits for the plurality of array groups, wherein the select circuit includes means for selectively forcing the qualified valid bits to a mismatch state according to priority; and

a priority encoder having a plurality of inputs to receive the plurality of qualified valid bits, and having an output to generate the NFA in response to the qualified valid bits.

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~~24~~. (Currently Amended) The CAM system of Claim ~~22~~ ~~23~~, wherein the select circuit passes only the valid bits from array groups having the same priority as the data, while disqualifying the valid bits from other array groups.

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~~25~~. (Currently Amended) The CAM system of Claim ~~22~~ ~~23~~,

wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the valid bits from a corresponding array group, a second input to receive an enable signal for the corresponding array group, and outputs to selectively provide the valid bits to the priority encoder as qualified valid bits in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priority of the data and the priorities of the array groups.

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~~26~~. (Original) The CAM system of Claim ~~25~~, wherein the compare circuit further comprises:

an input to receive the priority of the data; and

a table having a plurality of rows, each for storing the priority of a corresponding array group.

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~~27~~. (Currently Amended) The CAM system of Claim ~~22~~ ~~23~~, wherein the index circuit further comprises:

a group priority encoder having a plurality of inputs to receive a mask valid bit from each of the plurality of array groups, the mask valid bits indicating whether valid mask patterns are stored in corresponding group global masks of the array groups, and having an output to generate a first portion of the NFA for the data.

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~~28~~. (Original) The CAM system of Claim ~~27~~, wherein the index circuit further comprises a full flag circuit for generating a full flag in response to the qualified valid bits to indicate whether there are any available rows in array groups having the same priority as the data.

29. (Canceled)

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~~30~~. (Currently Amended) The CAM system of Claim ~~29~~ ~~33~~, wherein two or more array groups are assigned the same priority.

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~~31~~. (Currently Amended) The CAM system of Claim ~~29~~ ~~33~~, wherein each array group includes a group global register for storing a global mask pattern indicative of the priority of the array group.

32. (Canceled)

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~~33~~. (Currently Amended) ~~The CAM system of Claim 32,~~ A content addressable memory (CAM) system, comprising:

an array of binary CAM cells segmented into a plurality of array groups, each array group assigned a priority;

a plurality of group global masks, each for storing a mask pattern indicating priority of a corresponding array group;

a priority table including a plurality of rows, each for storing the priority of a corresponding array group; and

means for selectively comparing a search key with data stored in the array groups according to priority to generate a highest-priority match (HPM) index, wherein the means for selectively comparing comprises:

means for comparing the search key with data stored in each array group to generate match signals;

means for comparing a priority of the search key with the priority of each array group to generate enable signals; and

means for selectively allowing the match signals to participate in the generation of the HPM index in response to the enable signals.

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~~34~~. (Original) The CAM system of Claim ~~33~~, wherein the means for selectively allowing forces to a mismatch state the match signals of one or more array groups whose priority does not match the priority of the search key.

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~~35~~. (Original) The CAM system of Claim 33, wherein the means for selectively allowing allows the match signals of one or more array groups whose priority best matches the priority of the search key to participate in the generation of the HPM index.

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~~36~~. (Currently Amended) The CAM system of Claim ~~29~~ ~~33~~, further comprising:

means for storing data in the array groups according to priority.

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~~37~~. (Original) The CAM system of Claim ~~36~~, wherein the means for storing comprises:

means for generating a next free address (NFA) for each of a number of priorities;

an input to receive a priority for the data;

an NFA table having a number of rows, each for storing the NFA for a corresponding priority, the NFA table outputting the NFA indicated by the priority of the data; and

an address decoder for selecting a row in the array in response to the NFA provided by the NFA table.

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~~38~~. (Original) The CAM system of Claim ~~37~~, wherein each row in the NFA table includes an empty bit indicative of whether any array group is assigned to the corresponding priority.

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~~39~~. (Previously Amended) A method of operating a content addressable memory (CAM) system including an array of binary CAM cells segmented into a plurality of array groups, comprising:

assigning a priority to one or more array groups; and

selectively storing data in the array groups according to priority, wherein assigning the priority comprises:

for each array group, storing a mask pattern indicative of the priority assigned to the array group in a global mask for the array group; and

during compare operations between a comparand word and data stored in the array groups, masking the comparand word with corresponding mask patterns without comparing the mask patterns to the data stored in the corresponding array group.

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~~40~~. (Original) The method of Claim ~~39~~, wherein two or more array groups are assigned the same priority.

41. (Previously Canceled)

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~~42~~. (Original) The method of Claim ~~39~~, wherein the selectively storing data comprises:

receiving a priority of the data;

providing a next free address (NFA) corresponding to one of the array groups assigned to the priority of the data; and

storing the data in the array at the NFA.

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~~43~~. (Previously Amended) The method of Claim ~~42~~, wherein providing the NFA comprises:

generating an NFA for each priority;

storing the NFA for each priority in a corresponding row of

an NFA table;

selecting a row of the NFA table using the priority of the data; and

accessing the NFA corresponding to the priority of the data.

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~~44~~. (Original) The method of Claim ~~43~~, wherein generating the NFA comprises:

providing valid bits from each array group, the valid bits indicating whether valid data is stored in corresponding rows of each array group;

for each array group, comparing the priority of the data with the priority of the array group to generate an enable signal;

selectively allowing, in response to the enable signals, the valid bits from corresponding array groups to participate in the generation of the NFA.

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~~45~~. (Original) The method of Claim ~~44~~, wherein the selectively allowing comprises:

selectively qualifying the valid bits from each array group in response to the corresponding enable signal to generate qualified valid bits; and

generating the NFA in response to the qualified valid bits.

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~~46~~. (Currently Amended) The method of Claim ~~45~~, wherein selectively qualifying comprises:

forcing to a mismatch state the valid bits from each array group whose priority does not match the priority of the ~~search key~~ comparand word.

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~~47~~. (Currently Amended) The method of Claim ~~45~~, wherein

selectively qualifying comprises:

allowing the valid bits from each array group whose priority matches the priority of the ~~search key~~ comparand word to participate in the generation of the NFA.

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~~48~~. (Original) The method of Claim ~~43~~, wherein generating the NFA further comprises:

for each array group, storing a mask valid bit indicative of whether the array group is assigned to one of the priorities; and

generating a first portion of the NFA in response to the mask valid bits, the first portion of the NFA identifying one of the array groups that is not assigned to one of the priorities.

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~~49~~. (Original) The method of Claim ~~39~~, wherein the priority comprises a prefix of a classless inter-domain routing (CIDR) address.

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~~50~~. (Original) The method of Claim ~~49~~, further comprising:

generating an index of the longest prefix match in response to a comparison between a search key and data stored in the array groups.

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~~51~~. (Original) The method of Claim ~~39~~, further comprising:

selectively comparing a search key with data stored in the array groups according to priority.

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~~52~~. (Original) The method of Claim ~~51~~, wherein the selectively comparing comprises:

comparing the search key with data stored in the array

groups to generate match signals;

for each array group, comparing a priority of the search key with the priority of the array group to generate an enable signal; and

for each array group, selectively qualifying the match signals in response to the enable signal to generate qualified match signals.

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53. (Original) The method of Claim 52, wherein the selectively qualifying comprises:

forcing to a mismatch state the match signals for each array group whose priority does not match the priority of the search key.

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54. (Original) The method of Claim 52, wherein the selectively qualifying comprises:

enabling the match signals for each array group whose priority best matches the priority of the search key.

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55. (Original) The method of Claim 52, further comprising:

generating an index of the highest priority match (HPM) in response to the qualified match signals.

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56. (Original) The method of Claim 55, wherein the selectively qualifying comprises:

allowing the match signals from each array group whose priority best matches the priority of the search key to participate in the generation of the HPM index.

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57. (Original) The method of Claim 39, further comprising storing the priority for each array group in a priority table.

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~~58~~. (Previously Added) The CAM system of Claim 1, further comprising:

a plurality of mask valid bits, each mask valid bit indicating whether a corresponding group global mask stores a valid mask pattern.

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~~59~~. (Currently Amended) The CAM system of Claim ~~31~~ ~~38~~, further comprising:

a plurality of mask valid bits, each mask valid bit indicating whether a corresponding group global ~~register~~ mask stores a valid mask pattern.

60-62. (Canceled)

63. (Previously Canceled)

64-74. (Canceled)

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~~75~~. (Currently Amended) The CAM system of Claim ~~74~~ ~~80~~, wherein the means for storing further comprises an address circuit having a first input to receive the priority of the data, a second input to receive ~~a next free address (NFA) corresponding to the priority~~ the NFA, and having outputs coupled to the CAM array groups.

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~~76~~. (Previously Added) The CAM system of Claim ~~75~~, wherein the address circuit comprises an address decoder to select a row in one CAM array group corresponding to the priority in response to the NFA.

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~~77~~. (Previously Added) The CAM system of Claim ~~76~~, wherein the address circuit further comprises an NFA table having a number of rows, each row for storing the NFA for a

corresponding priority.

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~~78~~. (Previously Added) The CAM system of Claim ~~77~~, wherein each row in the NFA table includes an empty bit indicative of whether any CAM array group is assigned to the corresponding priority.

79. (Canceled)

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~~80~~. (Currently Amended) ~~The CAM system of Claim 79~~ A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells;

means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups; and

means for storing data in the CAM array groups according to priority, the means for storing data comprising an index circuit to generate a next free address (NFA) for the data according to its priority, wherein the index circuit comprises:

a select circuit having a plurality of inputs to receive valid bits from the plurality of CAM array groups, the valid bits indicating whether valid data is stored in corresponding rows of each CAM array group, and having a plurality of outputs to provide qualified valid bits for the plurality of CAM array groups; and

a priority encoder having a plurality of inputs to receive the qualified valid bits, and having an output to generate the NFA in response to the qualified valid bits.

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~~81~~. (Previously Added) The CAM system of Claim ~~80~~, wherein the select circuit includes means for selectively forcing the qualified valid bits to a mismatch state according to priority.

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~~82~~. (Previously Added) The CAM system of Claim ~~80~~, wherein the select circuit passes only the valid bits from CAM array groups having the same priority as the data, while disqualifying the valid bits from other CAM array groups.

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~~83~~. (Previously Added) The CAM system of Claim ~~80~~, wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the valid bits from a corresponding CAM array group, a second input to receive an enable signal for the corresponding CAM array group, and outputs to selectively provide the valid bits to the priority encoder as qualified valid bits in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priority of the data and the priorities of the CAM array groups.

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~~84~~. (Previously Added) The CAM system of Claim ~~83~~, wherein the compare circuit further comprises:

an input to receive the priority of the data; and

a table having a plurality of rows, each for storing the priority of a corresponding CAM array group.

85-88. (Previously Canceled)

89. (Canceled)

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~~90~~. (Currently Amended) The CAM device of Claim ~~89~~ ~~94~~, wherein the priority assigned to each array group is unrelated to the array group's location relative to the other array groups.

91. (Canceled)

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~~92~~. (Currently Amended) The CAM device of Claim ~~89~~ ~~94~~, further comprising:

an NFA table having a number of rows, each for storing the NFA for a corresponding priority.

93. (Canceled)

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~~94~~. (Currently Amended) ~~The CAM device of Claim 89~~ A content addressable memory (CAM) device, comprising:

a plurality of CAM array groups, each array group including a plurality of rows of CAM cells and a mask valid bit indicating whether the array group is assigned a priority relative to other array groups; and

an index circuit configured to generate a next free address (NFA) in response to the mask valid bits, wherein the index circuit further comprises:

a group priority encoder having inputs to receive the mask valid bits and having an output to generate a first portion of the NFA;

a select circuit having first inputs to receive ~~the~~ a plurality of valid bits indicating whether corresponding row contain valid data, a second input to receive a prefix value, and outputs to generate a plurality qualified valid bits; and

an array priority encoder having inputs to receive the qualified valid bits and having an output to generate a second portion of the NFA.

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~~95~~. (Previously Added) The CAM device of Claim ~~94~~, wherein the first portion of the NFA identifies an available array group and the second portion of the NFA identifies an available row in the available array group.

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~~96~~. (Previously Added) The CAM device of Claim ~~94~~, wherein the select circuit comprises:

a compare circuit having first inputs to receive priority information from the array groups, a second input to receive the prefix value, and outputs to generate a plurality of enable signals; and

a plurality of enable circuits, each having first inputs to receive the valid bits from a corresponding array group, a second input to receive a corresponding enable signal, and outputs to generate the qualified valid bits for a corresponding array group.

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~~97~~. (Previously Added) The CAM device of Claim ~~96~~, wherein the compare circuit further comprises a priority table having a plurality of rows, each for storing the priority of a corresponding array group.

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~~98~~. (Previously Added) The CAM device of Claim ~~94~~, further comprising an NFA table including:

a number of rows, each for storing the NFA for a corresponding priority;

a first input coupled to the output of the group priority encoder; and

a second input coupled to the output of the array priority encoder.

99-100. (Canceled)